

**QUARTZ CRYSTAL OSCILLATOR**
**■ GENERAL DESCRIPTION**

The NJU6374 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

This series are classed into three groups A to D, H to L and Q to T according to their oscillation frequency range mentioned in the line-up table.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors( $C_g$ ,  $C_d$ ), therefore, it requires no external component except quartz crystal.

The 3-stage divider generates  $f_o$ ,  $f_o/2$ ,  $f_o/4$  and  $f_o/8$  and only one frequency selected by internal circuits is output.

The 3-state output buffer is C-MOS compatible and capable of 10 LSTTL driving.

The NJU6374 series is suitable for the 3rd Over Tone and its pad location is the same as NJU6324 series.

**■ FEATURES**

- Operating Voltage. -- 4.0~6.0V
- Maximum Oscillation Frequency (See Line-Up Table)
- Low Operating Current
- High Fan-out -- LSTTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)  
Only one frequency out of  $f_o$ ,  $f_o/2$ ,  $f_o/4$  and  $f_o/8$  output
- Oscillation Capacitors  $C_g$  and  $C_d$  on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP/EMP 8
- C-MOS Technology

**■ LINE-UP TABLE**

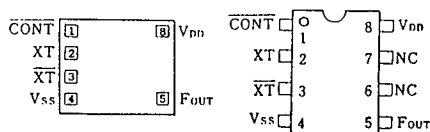
Type No.	Recommended Osc. Freq.	Output Freq.	$C_g, C_d$
NJU6374A 6374B 6374C 6374D	From 20 to 35MHz	$f_o$ $f_o/2$ $f_o/4$ $f_o/8$	28pF
NJU6374H 6374J 6374K 6374L	From 30 to 50MHz	$f_o$ $f_o/2$ $f_o/4$ $f_o/8$	20pF
NJU6374Q 6374R 6374S 6374T	From 45 to 75MHz	$f_o$ $f_o/2$ $f_o/4$ $f_o/8$	17pF

**■ PACKAGE OUTLINE**


NJU6374XC



NJU6374XE

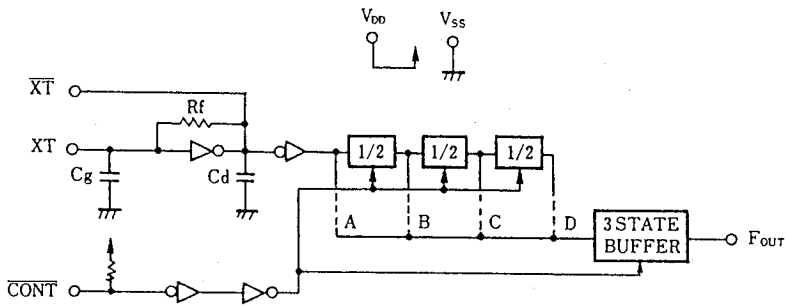
**■ PIN CONFIGURATION/PAD LOCATION**

**■ COORDINATES**

 Unit:  $\mu\text{m}$ 

No.	PAD	X	Y
1	CONT	-408	248
2	XT	-408	81
3	XT	-408	-86
4	VSS	-408	-248
5	FOUT	464	-248
6	NC	-	-
7	NC	-	-
8	VDD	464	248

Chip Size : 1.29 X 0.8mm  
 Chip Center : X=0 $\mu\text{m}$ , Y=0 $\mu\text{m}$   
 Chip Thickness : 400 $\mu\text{m}$ ±30 $\mu\text{m}$   
 (Note) No. 6 and 7 terminals are only for package type information. There are no PAD on the chip.

## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N	
1	$\overline{\text{CONT}}$	3-State Output Control and Divider Reset	
		$\overline{\text{CONT}}$	Output ( $F_{\text{OUT}}$ )
		H	Output either one frequency from $f_0$ , $f_0/2$ , $f_0/4$ and $f_0/8$
		L	Output High Impedance and Divider Reset
2	XT	Quartz Crystal Connecting Terminals	
3	$\overline{\text{XT}}$		
5	$F_{\text{OUT}}$	Output either one frequency from $f_0$ , $f_0/2$ , $f_0/4$ and $f_0/8$	
8	$V_{\text{DD}}$	+ 5V	
4	$V_{\text{SS}}$	GND	

**■ ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sub>DD</sub>	-0.5 ~ +7.0	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>O</sub>	-0.5 ~ V <sub>DD</sub> +0.5	V
Input Current	I <sub>IN</sub>	±10	mA
Output Current	I <sub>O</sub>	±25	mA
Power Dissipation (EMP)	P <sub>D</sub>	200	mW
Operating Temperature Range	Topr	-40 ~ + 85	°C
Storage Temperature Range	Tstg	-55 ~ +125	°C

(Note) Decoupling capacitor should be connected between V<sub>DD</sub> and V<sub>SS</sub> due to the stabilized operation for the circuit.

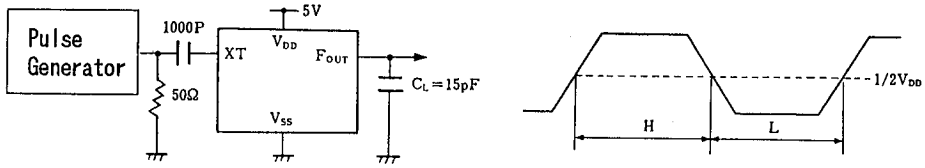
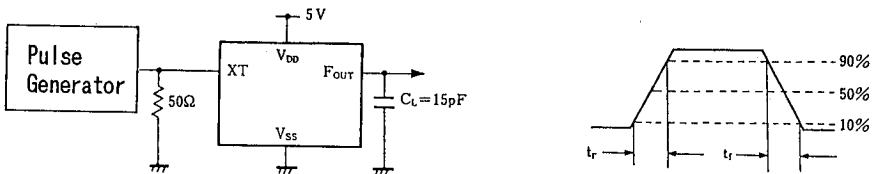
**■ ELECTRICAL CHARACTERISTICS**

 ( Ta=25°C, V<sub>DD</sub>=5V )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V <sub>DD</sub>		4		6	V
Operating Current	I <sub>DD1</sub>	A,B,C,D f <sub>OSC</sub> =24MHz, No Load			15	mA
	I <sub>DD2</sub>	H,J,K,L f <sub>OSC</sub> =48MHz, No Load			25	
	I <sub>DD3</sub>	Q,R,S,T f <sub>OSC</sub> =48MHz, No Load			28	
Stand-by Current	I <sub>st</sub>	CONT,XT=V <sub>SS</sub> , No Load (Note)			1	μA
Input Voltage	V <sub>IH</sub>		3.5		5.0	V
	V <sub>IL</sub>		0		1.5	
Output Current	I <sub>OH</sub>	V <sub>OH</sub> =4.5V	4			mA
	I <sub>OL</sub>	V <sub>OL</sub> =0.5V	4			
Input Current	I <sub>IN</sub>	CONT Terminal, CONT=V <sub>SS</sub>	125	250	500	μA
3-St Off-leakage Current	I <sub>oz</sub>	CONT=V <sub>SS</sub> , F <sub>OUT</sub> =V <sub>SS</sub> or V <sub>DD</sub>			±0.1	μA
Internal Capacitor	C <sub>g</sub> ,C <sub>d</sub>	A,B,C,D Version, f <sub>OSC</sub> =24MHz		28		pF
		H,J,K,L Version, f <sub>OSC</sub> =48MHz		20		
		Q,R,S,T Version, f <sub>OSC</sub> =48MHz		17		
Max. Oscillation Freq.	f <sub>MAX</sub>	A,B,C,D Version	35			MHz
		H,J,K,L Version	50			
		Q,R,S,T Version	75			
Output Signal Symmetry	SYM	C <sub>L</sub> =15pF at 1/2V <sub>DD</sub>	45	50	55	%
Output Signal Rise Time	t <sub>r</sub>	C <sub>L</sub> =15pF, 10% - 90%			6	ns
Output Signal Fall Time	t <sub>f</sub>	C <sub>L</sub> =15pF, 90% - 10%			6	ns

Note ) Excluding input current on CONT terminal.

## ■ MEASUREMENT CIRCUITS

 (1) Output Signal Symmetry ( $C_L=15\text{pF}$ )

 (2) Output Signal Rise / Fall Time ( $C_L=15\text{pF}$ )


# NJU6374 Series

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## MEMO

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